

Requested Patent: JP2001125937A

Title:

SYSTEM AND METHOD FOR DESIGNING LAYOUT OF SEMICONDUCTOR
INTEGRATED CIRCUIT DEVICE AND COMPUTER READABLE RECORDING
MEDIUM RECORDING PROGRAM FOR ALLOWING COMPUTER TO EXECUTE
RESPECTIVE MEANS IN THE SYSTEM OR RESPECTIVE PROCESSES IN THE
METHOD ;

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IPC Classification: G06F17/50 ; H01L21/82 ; H01L27/04 ; H01L21/822 ;

Equivalents:

ABSTRACT:

PROBLEM TO BE SOLVED: To automatically design a layout capable of reducing clock skew between layout blocks to a minimum in the case of designing a hierarchical layout having plural blocks. SOLUTION: After designing a floor plan and cell arrangement in each block, a clock tree is generated so that clock skew is minimized in each block of a lower hierarchy, the information of arrangement position of a route clock driver for each block and the information of an area capable of arranging cells are raised to an upper hierarchy, an average delay value from the route clock driver of each block up to a terminal buffer is found out in each block, and a clock tree is generated on the basis of these pieces of information so that clock skew between blocks on the upper hierarchy is minimized. Then the arrangement position of a newly generated buffer is adjusted on the basis of the cell arrangement of the corresponding block of the lower hierarchy to design wiring in each block and wiring between blocks.